REMARKS/ARGUMENTS

The Applicant thanks the Examiner for entering the Amendment filed on January 20, 2003 and for the Examiner's comments.

The Examiner objects to the drawings under 37 C.F.R. §1.83(a) for failing to show every feature of the invention specified in the claims. The Applicant traverses the rejection. A semiconductor die having a first major electrode of a first functionality disposed on a first major surface thereof and a second semiconductor die having a first major electrode of a first functionality disposed on a first major surface thereof and making electrical connections by wires are conventional features, which are disclosed in the description and claims. The Applicant suggests that a detailed illustration is not essential for a proper understanding of the invention. In addition, the wires are illustrated in Figs. 1 and 2 in the form of graphical drawing symbols for wires, and the semiconductor dies are included as a labeled representation. For example, a semiconductor die is shown in Fig. 1 as item 30, and a second semiconductor die is shown in Fig. 2 as item 31. The semiconductor dies are described in the specification in paragraphs 23, 24, and the wire bonding is described in paragraph 25 and 26. The wire bonds are shown in Figs. 1 and 2 as lines drawn from the semiconductor die to the various pins. Thus, the Applicant has complied with 37 C.F.R. §1.83. Applicant respectfully requests that the Examiner withdraw the objection.

The Examiner objects to claim 12 as lacking antecedent basis in the specification. However, the specification shows a first major electrode and a second major electrode in amended Fig. 2, which was amended in a previous response. Also, paragraph 24 recites "the source electrodes 30', 31' on the opposite surfaces of MOSFETs 30 and 31 and the gate electrodes 30", 31" on the same surfaces are then wire bonded to selected ones of the lead frame pins." The terms "a first major electrode" and "a second major electrode" merely distinguish electrodes such as 30', 31' from the control electrodes, such as 30" and 31" which are claimed in dependent claim 14. Thus, the term "a first major electrode" merely refers to a conventional electrode disposed on a first major surface, compared to a control electrode on a second major surface. Thus, the Applicant believes that there is sufficient support and antecedent basis in the specification and drawings for the terms "a first major electrode" and "a second major electrode."

Applicant respectfully requests that the Examiner withdraw the objection for failing to provide proper antecedent basis for the claimed subject matter.

The Examiner objects to claims 10 and 17 based on informalities. Please cancel claim 10, which the Applicant intended to cancel in the Amendment accompanying the Request for Continued Examination. Claim 17 has been amended to correct the typographical error identified by the Examiner.

Claims 10, 12, 15, 18 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Golwalkar et al. in view of Kim. However, neither Golwalkar et al. nor Kim teaches or discloses each and every element of the claimed invention. On page 5 of the Office Action, in the paragraph that starts "Kim does not disclose a first semiconductor die ...," the Applicant assumes that the Examiner meant "Golwalkar et al. does not disclose ...." If so, then the Examiner states that Golwalkar et al. does not disclose a first semiconductor die being electrically connected to said first major surface of said conductive die and a second semiconductor die being electrically connected to said second major surface of said conductive die pad.

Furthermore, Kim does not teach use of a die pad. Instead, Kim teaches flip chip bonding between a semiconductor chip and an interface board, which is a printed circuit board (PCB). For example, in column 5, lines 50-54, the "flip chip bonding between the interface board and the semiconductor chips is a bonding process in which bonding is carried out on a PCB, and therefore, the bonding becomes easy, so that a mass production may be possible." If the interface board of Kim were a conductive die pad, as that term is known in the art, then the device shown in Fig. 2 is non-functional. Specifically, all of the leads connected by the plurality of interface board bump pads would be electrically connected, one to the other. Thus, the semiconductor die's connections would be shorted. Therefore, Kim teaches away from electrically connecting a second major surface and a first major surface of the conductive die pad to each of a first major electrode of a first semiconductor die and a first major electrode of a second semiconductor die.

Thus, neither Golwalkar et al. nor Kim teaches a first semiconductor die having a first major electrode of a first functionality and a second semiconductor die having a first major electrode of a first functionality, said first major electrode of said first semiconductor die and

said first major electrode of said second semiconductor die being electrically connected to said first major surface of said conductive die pad. As neither Golwalkar et al. nor Kim, either alone or in combination, teaches each and every element of the invention; therefore, the combination fails to establish *prima facie* obviousness under 35 U.S.C. §103.

Arguendo, even if the Examiner believes that a *prima facie* case exists for obviousness, Kim teaches away from the use of a conductive die pad, as that term is known in the art. Thus, there is no motivation to combine Golwalkar et al. and Kim, and claim 12 is nonobvious.

Claims 15, 18 and 19 depend from claim 12, incorporating all of the limitations of claim 12, therefore, claims 12, 15, 18 and 19 are nonobvious over Golwalkar et al. and Kim.

Claims 13, 14 and 16 are rejected under 35 U.S.C. §103(a) as unpatentable over Golwalkar et al. and Kim as applied to claim 12 above and further in view of Munoz et al. Although claims 13, 14 and 16 are rejected based on the additional teachings of Munoz et al., the Applicant suggests that the additional teachings neither teach nor suggest the limitations missing from Golwalkar et al. and Kim. Specifically, Munoz et al. merely teaches the conventional bonding of a MOSFET to a copper lead frame, using an improved ultrasonically-scrubbed soldering technique. Therefore, the applied prior art fails to establish *prima facie* obviousness under 35 U.S.C. §103, and claims 13, 14 and 16 are nonobvious over the cited references.

Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Golwalkar et al., Kim and Munoz et al. as applied to claims 12-14 above and further in view of Adishian. Adishian does not show a die pad, as that term is known in the art. Instead, Adishian shows transistors mounted on a flange (column 2, lines 5-8). The additional teachings of Adishian neither teach nor suggest the limitations missing from Golwalkar et al., Kim and Munoz et al.; therefore, the applied prior art fails to establish *prima facie* obviousness under 35 U.S.C. §103.

The Applicant requests that the Examiner reconsider the application and allow all of the pending claims, claims 12-19.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 3, 2003:

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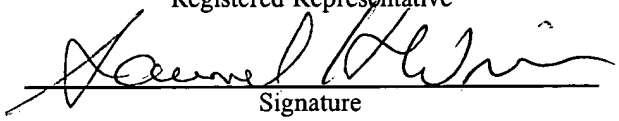
Name of applicant, assignee or Registered Representative



Signature

July 3, 2003

Date of Signature

Respectfully submitted,

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